

Notice of References Cited	Application/Control No. 09/896,059	Applicant(s)/Patent Under Reexamination BHATTACHARYA ET. AL.	
	Examiner A. M. Thompson	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,301,692	10-2001	Kumashiro et al.	716/10
	B	US-6,051,031	04-2000	Shubat et al.	716/3
	C	US-5,923,569	07-1999	Kumashiro et al.	716/7
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Premal Buch et al., Logic Synthesis for Large Pass Transistor Circuits, IEEE/ACM International Conference on Computer-Aided Design, pages 663-670, November 1997
	V	R. Murgai et al., Sequential Synthesis for Table Look Up PGA's, Proceedings of Euro ASIC '92, pages 32-37, June 1992.
	W	E.M. Sentovich et al., SIS: A System for Sequential Circuit Synthesis, Electronics Research Library, University of California, Berkeley, 1992, pages 1-45
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.